**Module:** Telescopic Cascode Operational Amplifier

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**Date:** 1st May 2019

**Module Description:** Telescpoic Cascode Operational Amplifier utilizes the cascode topology on the pull down and pull up at the same time to achieve high gain and high speed, while sacrifices the swing and input common mode range.

**Top Cell Name:** AMP\_CASCODE65\_v1

**Technology:** TSMC 65nm CMOS

**PINS:**

|  |  |
| --- | --- |
| Pin Lists |  |
| VDD | Supply Voltage |
| VSS | Ground |
| TP, TP2, TN2, T | Bias voltages |
| IM, IP | Input Differential Voltage |
| OM, OP | Output Differential Voltage |

**Schematic Netlists:** ATC\_v1.scs

**Schematic figures:**

A screenshot of a cell phone

Description generated with very high confidence

**Testbenches:** ATC\_test.scs

**Parameters:**

|  |  |
| --- | --- |
| Parameters | Symbols |
| Top PMOS # of Fingers |  |
| Top PMOS Length (m) |  |
| Mid PMOS # of Fingers |  |
| Mid PMOS Length (m) |  |
| Mid NMOS # of Fingers |  |
| Mid NMOS Length (m) |  |
| Bot NMOS # of Fingers |  |
| Bot NMOS Length (m) |  |
| Sink NMOS # of Fingers |  |
| Sink NMOS Length (m) |  |
| Sink NMOS Bias (V) |  |
| Common Mode Voltage (V) |  |
| Mid NMOS Bias (V) |  |
| Mid PMOS Bias (V) |  |
| Output Capacitive Load (F) |  |

**Metrics:**

|  |  |
| --- | --- |
| Metrics | Symbols |
| DC Power Consumption (W) | power |
| Output Swing Voltage (V) | swing |
| Common mode voltage gain (dB) | avcm |
| Differential gain (dB) | avd |
| Input Capacitance (F) | cin |
| Unity Gain Bandwidth (Hz) | gbw |
| Output Noise (V^2/Hz) | outnoise |

**Neural Network Model:**

**The H5 file:** reg\_ATC65.h5

**The Json File:** model\_ATC65.json

**The Input Normalization File:** scX\_ATC65.pkl

**The Output Standardization File:** scY\_ATC65.pkl

**The input characterization range of the Model:**

|  |  |
| --- | --- |
| Design parameters |  |
| Symbols | Characterization Range |
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Another parameter ranges:

|  |  |  |
| --- | --- | --- |
| Design parameters |  |  |
| Symbols | Description | Characterization Range |
|  | Supply Voltage |  |
|  | Top PMOS Width |  |
|  | Mid PMOS Width |  |
|  | Mid NMOS Width |  |
|  | Bot NMOS Width |  |
|  | Sink NMOS Width |  |
|  | Output loading resistance |  |
|  | Loading DC voltage |  |
|  | Output Common Mode Voltage |  |

**The estimation error over the metrics:**







